DACs Connection Detection of CH7xxx Encoders

1. Introduction

This application note explains the DACs connection detection method used in Chrontel CH7xxx Encoders. CH7xxx includes CH7009-7012, CH7015, CH7017, CH7019, CH7205, and CH7301 devices. For those Chrontel encoders not mentioned above, please contact Chrontel Applications Group for details.

2. DACs Connection Detection

In order to make a proper display on a display device, the encoder's DACs connection detection procedure may first be completed. Then, depending on which DACs have sensed a connection, the encoder will drive out the corresponding video signals from the connected DACs.

2.1 DAC Connection Detection Procedure

Connection Detect (CD) Register (Register 20h)

Bit	7	6	5	4	3	2	1	0
SYMBOL	X	X	X	DACT3	DACT2	DACT1	DACT0	SENSE
TYPE	X	X	X	R	R	R	R	R/W
DEFAULT:	X	X	X					0

DAC Control (DC) Register (Register 21h)

Bit	7	6	5	4	3	2	1	0
SYMBOL	X	X	X	X	X	X	X	DACBP
TYPE	X	X	X	X	X	X	X	R/W
DEFAULT:	X	X	X	X	X	X	X	0

The DACT[3:0] (bits 4-1) and SENSE (bit 0) bits of Register CD provide a means to sense the connection of a display device. The status bits, DACT[3:0] corresponds to the resistive load present on each of the four corresponding DAC outputs. However, the values contained in these status bits ARE NOT VALID until the sensing procedure has been performed. Use of this Register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits.

The connection detection procedure is as follows:

1. Enable all DACs by setting the Power Management Register, Register 49h, accordingly.
2. Verify that the value of the DACBP bit of the DAC Control (DC) Register, Register 21h - bit 0 is '0' (Bypass mode is disabled).
3. Set the SENSE bit of the Connection Detect (CD) Register, Register 20h - bit 0 to '1'. This forces a constant DC current output from the DACs. Note that when SENSE = '1', all 4 DACs send out a DC current and no horizontal/vertical sync pulses are asserted.
4. Reset the SENSE bit to '0'. This triggers a comparison between the voltage present on a corresponding DAC pin and the internal reference voltage is used as a threshold. During this step, each of the four DAC status bits that corresponds to the individual DAC output will be set to '0' if it is NOT CONNECTED, and '1' if it is CONNECTED.

5. Read the status bits. The status bits, DACT[3:0], now contain valid information which can be read to determine which DACs are connected externally. A ’1’ indicates a valid connection and a ’0’ indicates an unconnected DAC.

2.2 Explanation of the Flash on the Display Device During the Detection Process

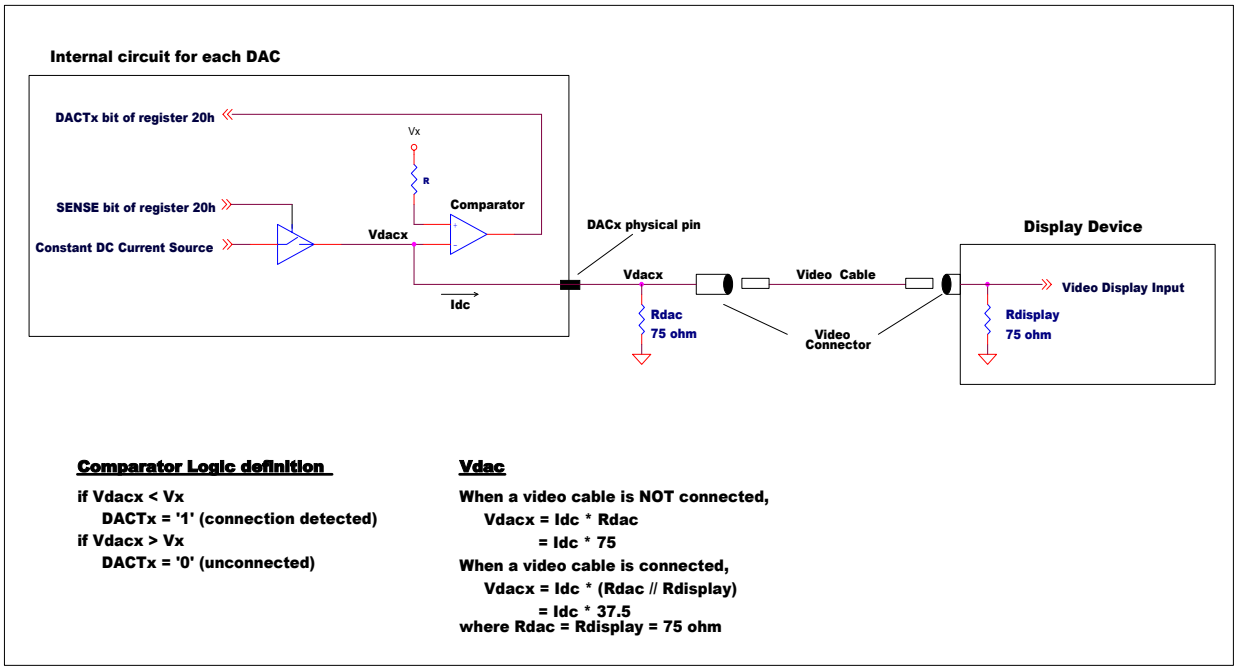

Figure 1: Connection Detection Diagram

Figure 1 illustrates why the display device will flash. The flash is due to the small constant DC current that is driven out of the DACs and flows into the connected display device during the connection detection process. This symptom is normal and will not cause any damage to the connected display device.

3. Revision History

Revision	Date	Section	Description
1.0	7/30/03	All	First official release, Revision 1.0

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